UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,037	08/15/2001	Toru Koizumi	35.C15698	1876

5514 7590 01/24/2007

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
QUIETT, CARRAMAH J	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/929,037	KOIZUMI ET AL.	
	Examiner	Art Unit	
	Carramah J. Quiett	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *9-16 and 21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,17-20 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment(s), filed on 11/06/2006, have been entered and made of record. Claims 1-27 are pending, of which claims 9-16 and 21-24 are withdrawn from consideration.

Response to Arguments

2. Applicant's arguments filed 11/06/2006 have been fully considered but they are not persuasive.

For **claim 1**, Applicant asserts that Masuyama does not teach the applicant's invention as claimed. Examiner *respectfully* disagrees. Claim 1 now recites the following limitation, "...wherein said drive circuit (inherently) controls to hold the third signal level for a part of a time period after an end of an accumulation period of accumulating a carrier in the photoelectric conversion unit until a start of transferring the signal from the photoelectric conversion unit while said transfer switch is changing from the ON state to the OFF state." In col. 11, line 51 – col. 12, line 4, Masuyama inherently teaches the limitations in claim 1 because charges are not transferred unless the charges have been accumulated. Also, please see the timing chart in figure 15.

For **claim 5**, Applicant asserts that Hamasaki as modified by Suzuki does not teach a signal for controlling said transfer switch so that a time during which said transfer switch changes from an ON state to an OFF state becomes longer than a time during which said transfer switch changes from the OFF state to the ON state. Respectfully, the examiner disagrees. Suzuki illustrates a *time* chart in fig. 4 and teaches the detail of fig. 4 in col. 9, lines 15-63. From t_3-t_7, transfer pulse V_3 goes from a high voltage (V_H) to an intermediate voltage (V_M) and then a low

voltage (V_L) at t_7. Then at t8, V_3 goes from V_L to V_H without a V_M. Please read col. 8, lines 11-23 and col. 9, lines 15-63.

3. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., an operation of transferring an accumulated carrier after the end of a carrier accumulation period for a photoelectric conversion element) are not recited in the rejected **claim 25**. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. Accordingly, the previous rejections to claims 1-8, 17-20, 25, 26 and 27 are maintained.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 1-3 and 25** are rejected under 35 U.S.C. 102(e) as being anticipated by Masuyama (U.S. Pat. #6,674,471).

For **claim 1**, Masuyama discloses an image pickup device (figs. 1-2) comprising:

a plurality of pixels (fig. 1, ref. 1; col. 4, lines 54-67) each including a photoelectric conversion unit (fig. 2, ref. 3; col. 5, lines 1-2), a semiconductor area (fig. 2, ref. 5) to which a signal from said photoelectric conversion unit is transferred (col. 5, lines 1-25), a transfer switch (fig. 2, ref. 4) to transfer the signal from said photoelectric conversion unit to said semiconductor area (col. 5, lines 1-25), and a read unit (fig. 2, refs. 6a/b) to read out the signal from said semiconductor area (col. 5, line 26-47); and

a drive circuit (fig. 1, refs. 41/42) coupled to said pixels (col. 5, line 59 – col. 6, line 3) and to output a first signal level at which said transfer switch is set in an OFF state (col. 11, lines 22-32), a second signal level at which said transfer switch is set in an ON state (col. 11, lines 51-59), and a third signal level between the first level and the second level (col. 11, lines 33-50),

wherein said drive circuit (inherently) controls to hold the third signal level for a part of a time period after an end of an accumulation period of accumulating a carrier in the photoelectric conversion unit until a start of transferring the signal from the photoelectric conversion unit while said transfer switch is changing from the ON state to the OFF state (col. 11, line 51 – col. 12, line 4). Also, please see the timing relationship for TRi in figs. 11 and 15.

For **claim 2**, Masuyama discloses a device wherein said read unit includes an amplification transistor (fig. 2, ref. 6a) for amplifying and outputting the signal in said semiconductor area (col. 5, line 26-47).

For **claim 3**, Masuyama discloses a device wherein said photoelectric conversion unit includes an embedded photodiode (col. 5, lines 1-12).

Regarding **claim 25**, this claim is a method claim, which has very similar limitations as claimed in the apparatus claim 1. Therefore, claim 25 is analyzed and rejected as previously discussed with respect to claim 1.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuyama (U.S. Pat. #6,674,471) in view of Gowda et al. (U.S. Patent #6,344,877).

For **claim 4**, Masuyama discloses a solid-state imaging device in fig. 1. However, Masuyama does not expressly discloses a device further comprising

an analog/digital conversion circuit to convert a signal from each of said plurality of pixels into a digital signal, a signal processing circuit to process the signal from said analog/digital conversion circuit, and a recording circuit to record the signal processed by said signal processing circuit.

In a similar field of endeavor Gowda discloses a device further comprising an analog/digital conversion circuit (fig. 2, ref. 52) to convert a signal from each of said plurality of pixels into a digital signal (col. 4, lines 12-15), a signal processing circuit (fig. 2, ref. 44) to process the signal from said analog/digital conversion circuit (col. 4, lines 59-61), and a recording circuit (fig. 2, after ref. 44) to record the signal processed by said signal processing circuit – inherently, because after ref. 44 (col. 4, lines 59-61), the image signals are transferred to processing/image storage electronics. Please see fig. 2. In light of the teachings of Gowda, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Masuyama to include an analog/digital conversion circuit, a signal processing circuit, and a recording circuit in order to further process an enhanced image.

9. **Claims 5-8 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki et al. (U.S. Patent #5,187,583) in view of Suzuki et al. (U.S. Patent #5,828,407).

For **claim 5**, Hamasaki discloses an image pickup device (fig. 1) comprising:

a plurality of pixels (ref. 5 – FDA) each including a photoelectric conversion unit (fig. 1, not numbered; (col. 3, lines 8-19), a semiconductor area (1 – ST) to which a signal from said photoelectric conversion unit is transferred (col. 3, lines 21-35), a transfer switch (2 – OG) to transfer the signal from said photoelectric conversion unit to said semiconductor area (col. 3, lines 21-35), and a read unit (ref. 4) to read out the signal from said semiconductor area (col. 3, lines 21-35); and

a drive circuit coupled to said pixels (ref. 8; col. 3, lines 20-39).

However, Hamasaki does not expressly disclose a drive circuit to output a signal for controlling said transfer switch so that a time during which said transfer switch changes from an ON state to an OFF state becomes longer than a time during which said transfer switch changes from the OFF state to the ON state.

In a similar field of endeavor, Suzuki discloses a transfer switch (fig. 1, refs. 10/11; col. 7, lines 7-14) and a drive circuit (fig. 1, refs. 2-4; col. 6, lines 58-65) to output a signal for controlling said transfer switch so that a time during which said transfer switch changes from an ON state to an OFF state becomes longer than a time during which said transfer switch changes from the OFF state to the ON state (col. 9, lines 15-63). Also in Suzuki, please see figs. 3-5. In light of the teaching of Suzuki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the driving circuit of Hamasaki in order to improve the dynamic range of the image thereby realizing high charge transfer efficiency without causing blooming (Suzuki, col. 4, lines 49-56).

For **claim 6**, Hamasaki, as modified by Suzuki, discloses a device wherein said read unit includes an amplification transistor (fig. 2, ref. 4) for amplifying and outputting the signal in said semiconductor area (col. 3, line 8-19).

For **claim 7**, Hamasaki, as modified by Suzuki, Hamasaki teaches an embedded photodiode in a photoelectric conversion unit (fig. 1; col. 3, line 8-19).

For **claim 8**, Hamasaki, as modified by Suzuki, discloses a device (Suzuki, fig. 1) further comprising an analog/digital conversion circuit (ref. 6) to convert a signal from each of said plurality of pixels into a digital signal (col. 7, lines 1-3), a signal processing circuit (ref. 7) to process the signal from said analog/digital conversion circuit (col. 7, lines 1-5), and a recording circuit (ref. 9) to record the signal processed by said signal processing circuit (col. 7, lines 1-7).

Regarding **claim 26**, this claim is a method claim corresponding to the apparatus claim 5. Therefore, claim 26 is analyzed and rejected as previously discussed with respect to claim 5.

10. **Claims 17-20 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (U.S. Patent #6,344,877).

For **claim 17**, Gowda discloses an image pickup device (fig. 2) comprising:

a plurality of pixels (fig. 2, ref. 30; col. 4, lines 1-7) each including a photoelectric conversion unit (fig. 3, ref. 26), a semiconductor area to which a signal from said photoelectric conversion unit is transferred (col. 4, line 62 – col. 5, line 18), a transfer switch (fig. 3, ref. 22) to transfer the signal from said photoelectric conversion unit to said semiconductor area (col. 5, lines 19-59), and a read unit (fig. 3, ref. 23) to read out the signal from said semiconductor area (col. 5, line 50-59); and a drive circuit coupled to said pixels (fig. 2, ref. 14; col. 4, lines 27-62)

and to output a signal to control said transfer switch so that a fall speed V_{off} for changing said transfer switch from an ON state to an OFF state has a relation 1.2, 1.8, 2.5, 3.3, or 5 volts on the order of 2μsec (col. 7, lines 16-23 and col. 8, lines 29-40).

However, Gowda does not expressly teach that changing said transfer switch from an ON state to an OFF state has a relation 10 V/μsec>V_{off}.

The Examiner takes Official Notice that it is well known in the art for a drive circuit to output a signal to control a transfer switch so that a fall speed V_{off} for changing the transfer switch from an ON state to an OFF state has a relation 10 V/μsec>V_{off}. *It is noted by the Examiner that because Applicant failed to timely traverse the old and well-known statement, it is now taken as Admitted Prior Art (see MPEP 2144.03(c)).* Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the driving circuit of Gowda in order to facilitate high-speed imaging.

For **claim 18**, Gowda discloses a device wherein said read unit includes an amplification transistor (fig. 3, ref. 23) for amplifying and outputting the signal in said semiconductor area (col. 5, lines 50-59).

For **claim 19**, Gowda discloses a device wherein said photoelectric conversion unit includes an embedded photodiode (fig. 3, ref. 26; col. 4, line 62 – col. 5, line 18).

For **claim 20**, Gowda discloses a device further comprising

an analog/digital conversion circuit (fig. 2, ref. 52) to convert a signal from each of said plurality of pixels into a digital signal (col. 4, lines 12-15).

a signal processing circuit (fig. 2, ref. 44) to process the signal from said analog/digital conversion circuit (col. 4, lines 59-61), and

a recording circuit (fig. 2, after ref. 44) to record the signal processed by said signal processing circuit – inherently, because after ref. 44 (col. 4, lines 59-61), the image signals are transferred to processing/image storage electronics. Please see fig. 2.

Regarding **claim 27**, this claim is a method claim corresponding to the apparatus claim 17. Therefore, claim 27 is analyzed and rejected as previously discussed with respect to claim 17.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CJQ
January 19, 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER